ABSTRACT

The present invention relates to a method of manufacturing a NAND flash memory device. Drain select transistors, source select transistors and memory cells are formed in a cell region. After forming peri-transistors in a peripheral circuit region, a metal contact process for electrically connecting them is performed. Upon the metal contact process, the common source line connecting a source region of each of the source select transistors is formed, by patterning the interlayer insulating film to expose the source regions, removing the isolation films between respective source regions to form a common source line contact hole, forming an ion implantation region in the semiconductor substrate at the bottom of the common source line contact hole by means of an ion implantation process, forming a conductive layer so that the common source line contact hole is filled, and blanket-etching the interlayer insulating film as well as the conductive layer by a given thickness. The common source line has a reduced electrical resistance that much since the conductive layer is buried into the removed portion of the isolation film as well as the impurity region formed by the ion implantation process. Due to this, the height of the interlayer insulating film relating to the resistance of the common source line can be lowered. As a result, the aspect ratio is reduced to facilitate a subsequent contact process.